

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT373

**Octal D-type transparent latch;
3-state**

Product specification
File under Integrated Circuits, IC06

September 1993

Octal D-type transparent latch; 3-state

74HC/HCT373

FEATURES

- 3-state non-inverting outputs for bus oriented applications
- Common 3-state output enable input
- Functionally identical to the “563”, “573” and “533”
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT373 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT373 are octal D-type transparent latches featuring separate D-type inputs for each latch and 3-state outputs for bus oriented applications. A latch enable (LE)

input and an output enable (\overline{OE}) input are common to all latches.

The “373” consists of eight D-type transparent latches with 3-state true outputs. When LE is HIGH, data at the D_n inputs enters the latches. In this condition the latches are transparent, i.e. a latch output will change state each time its corresponding D-input changes.

When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE. When \overline{OE} is LOW, the contents of the 8 latches are available at the outputs. When \overline{OE} is HIGH, the outputs go to the high impedance OFF-state. Operation of the \overline{OE} input does not affect the state of the latches.

The “373” is functionally identical to the “533”, “563” and “573”, but the “563” and “533” have inverted outputs and the “563” and “573” have a different pin arrangement.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns

| SYMBOL | PARAMETER | CONDITIONS | TYPICAL | | UNIT |
|-------------------------------------|---|---|---------|-----|------|
| | | | HC | HCT | |
| t _{PHL} / t _{PLH} | propagation delay | C _L = 15 pF; V _{CC} = 5 V | | | |
| | D _n to Q _n | | 12 | 14 | ns |
| | LE to Q _n | | 15 | 13 | ns |
| C _I | input capacitance | | 3.5 | 3.5 | pF |
| C _{PD} | power dissipation capacitance per latch | notes 1 and 2 | 45 | 41 | pF |

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz

f_o = output frequency in MHz

∑ (C_L × V_{CC}² × f_o) = sum of outputs

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

2. For HC the condition is V_I = GND to V_{CC}. For HCT the condition is V_I = GND to V_{CC} – 1.5 V

ORDERING INFORMATION

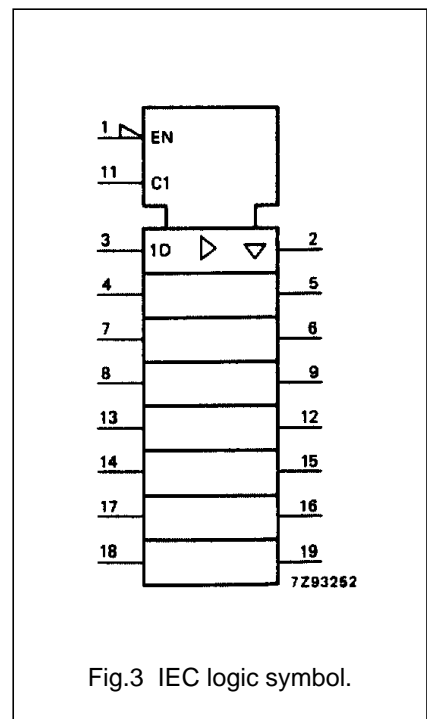
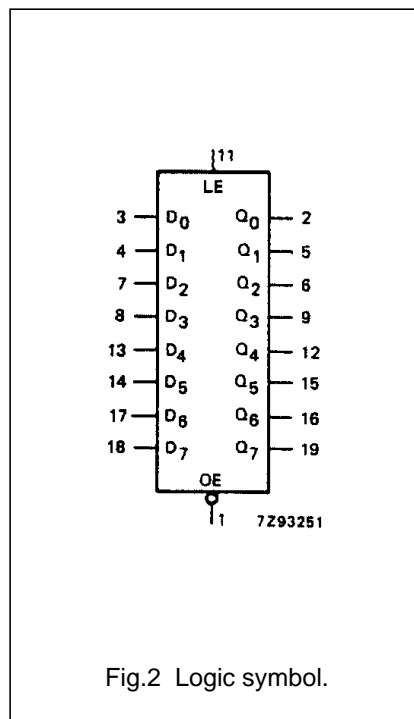
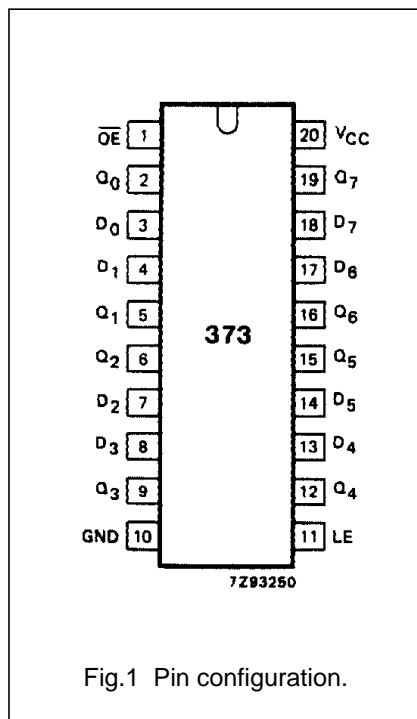
See “74HC/HCT/HCU/HCMOS Logic Package Information”.

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PIN DESCRIPTION

| PIN NO. | SYMBOL | NAME AND FUNCTION |
|----------------------------|-----------------|--|
| 1 | \overline{OE} | 3-state output enable input (active LOW) |
| 2, 5, 6, 9, 12, 15, 16, 19 | Q_0 to Q_7 | 3-state latch outputs |
| 3, 4, 7, 8, 13, 14, 17, 18 | D_0 to D_7 | data inputs |
| 10 | GND | ground (0 V) |
| 11 | LE | latch enable input (active HIGH) |
| 20 | V_{CC} | positive supply voltage |



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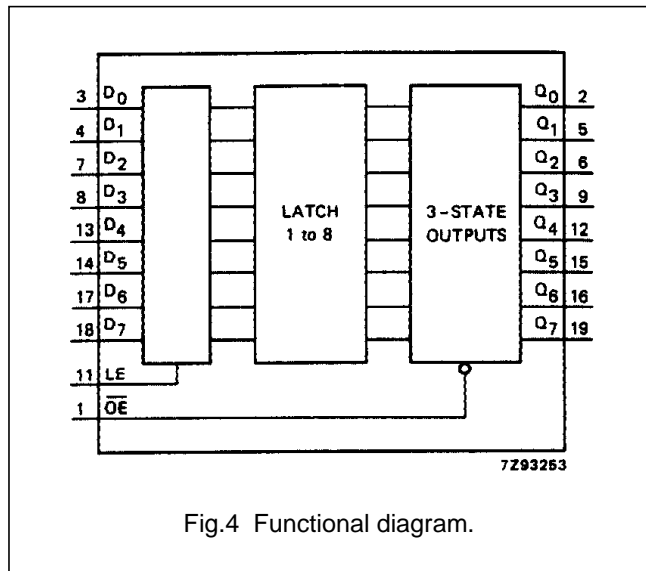


Fig.4 Functional diagram.

FUNCTION TABLE

| OPERATING MODES | INPUTS | | | INTERNAL LATCHES | OUTPUTS Q ₀ to Q ₇ |
|---|-----------------|----|----------------|------------------|---|
| | \overline{OE} | LE | D _n | | |
| enable and read register (transparent mode) | L | H | L | L | L |
| enable and read register (transparent mode) | L | H | H | H | H |
| latch and read register | L | L | l | L | L |
| latch and read register | L | L | h | H | H |
| latch register and disable outputs | H | X | X | X | Z |
| latch register and disable outputs | H | X | X | X | Z |

Notes

- H = HIGH voltage level
 h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition
 L = LOW voltage level
 l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition
 X = don't care
 Z = high impedance OFF-state

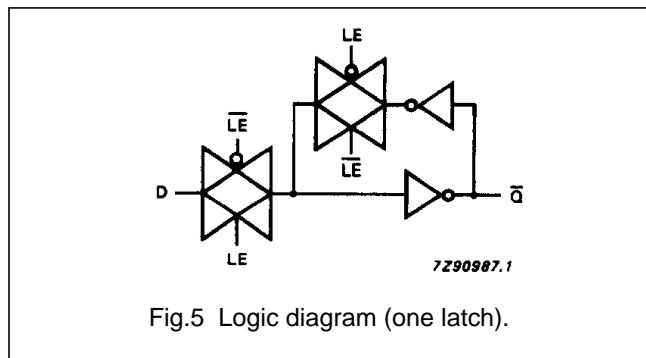


Fig.5 Logic diagram (one latch).

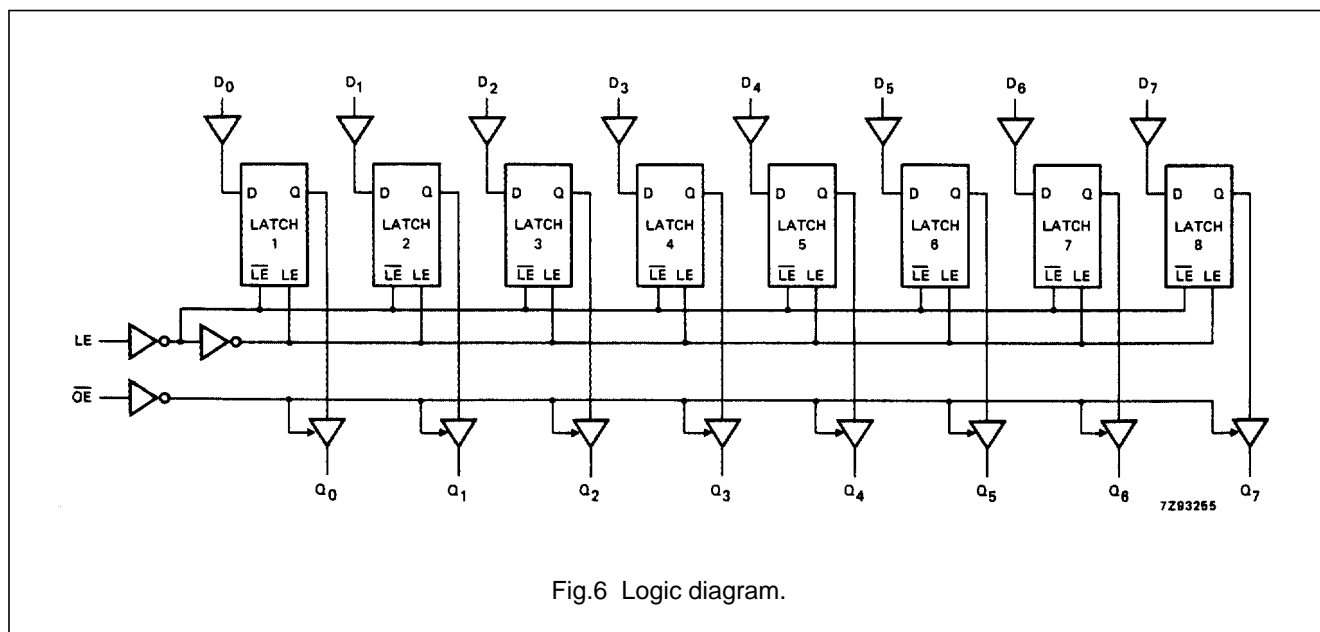


Fig.6 Logic diagram.

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DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

| SYMBOL | PARAMETER | T _{amb} (°C) | | | | | | UNIT | TEST CONDITIONS | | |
|-------------------------------------|--|-----------------------|----------------|-----------------|-----------------|-----------------|-----------------|-----------------|------------------------|-------------------|--------|
| | | 74HC | | | | | | | V _{CC} (V) | WAVEFORMS | |
| | | +25 | | | -40 to +85 | | -40 to +125 | | | | |
| | | min. | typ. | max. | min. | max. | min. | | | | max. |
| t _{PHL} / t _{PLH} | propagation delay D _n to Q _n | | 41 15 12 | 150 30 26 | | 190 38 33 | | 225 45 38 | ns | 2.0 4.5 6.0 | Fig.7 |
| t _{PHL} / t _{PLH} | propagation delay LE to Q _n | | 50 18 14 | 175 35 30 | | 220 44 37 | | 265 53 45 | ns | 2.0 4.5 6.0 | Fig.8 |
| t _{PZH} / t _{PZL} | 3-state output enable time \overline{OE} to Q _n | | 44 16 13 | 150 30 26 | | 190 38 33 | | 225 45 38 | ns | 2.0 4.5 6.0 | Fig.9 |
| t _{PHZ} / t _{PLZ} | 3-state output disable time \overline{OE} to Q _n | | 47 17 14 | 150 30 26 | | 190 38 33 | | 225 45 38 | ns | 2.0 4.5 6.0 | Fig.9 |
| t _{THL} / t _{TLH} | output transition time | | 14 5 4 | 60 12 10 | | 75 15 13 | | 90 18 15 | ns | 2.0 4.5 6.0 | Fig.7 |
| t _W | LE pulse width HIGH | 80 16 14 | 17 6 5 | | 100 20 17 | | 120 24 20 | | ns | 2.0 4.5 6.0 | Fig.8 |
| t _{su} | set-up time D _n to LE | 50 10 9 | 14 5 4 | | 65 13 11 | | 75 15 13 | | ns | 2.0 4.5 6.0 | Fig.10 |
| t _h | hold time D _n to LE | 5 5 5 | -8 -3 -2 | | 5 5 5 | | 5 5 5 | | ns | 2.0 4.5 6.0 | Fig.10 |

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DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

| INPUT | UNIT LOAD COEFFICIENT |
|-----------------|-----------------------|
| D _n | 0.30 |
| LE | 1.50 |
| \overline{OE} | 1.00 |

AC CHARACTERISTICS FOR 74HCT

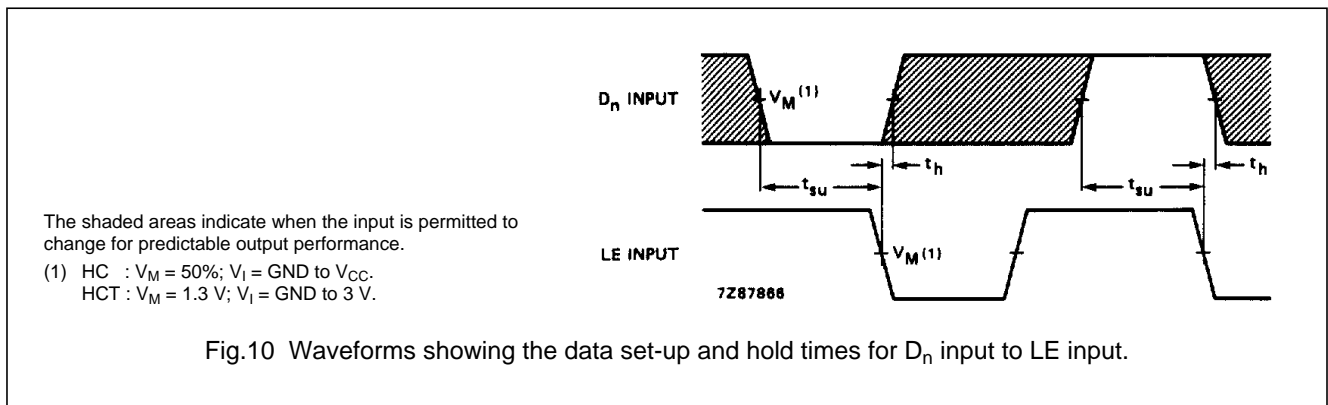
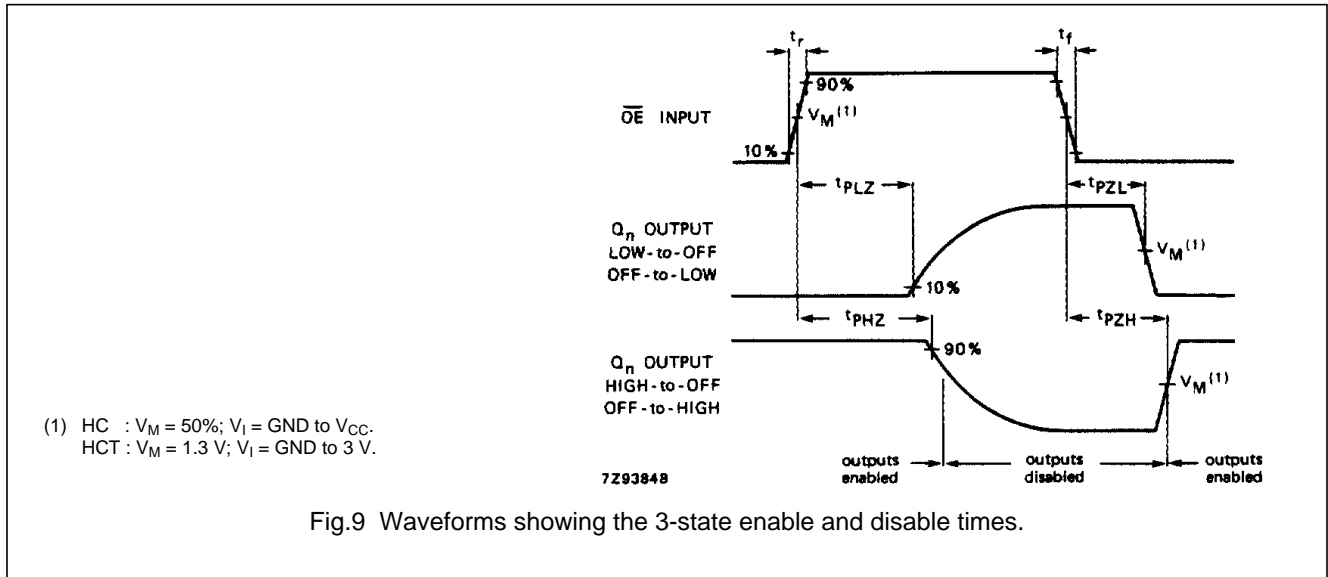
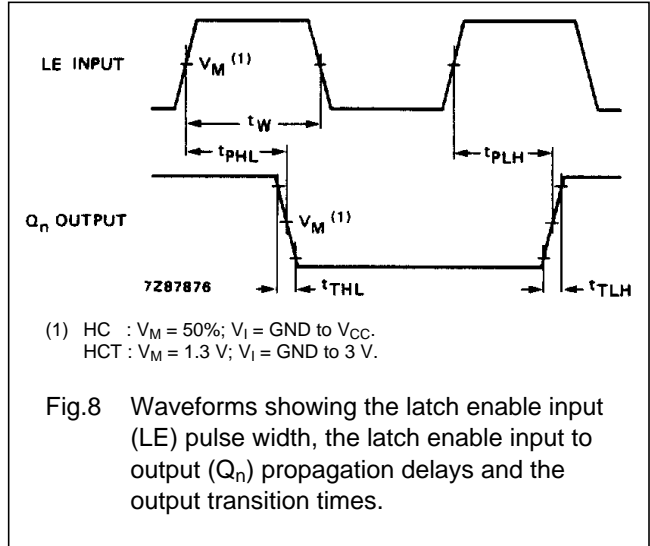
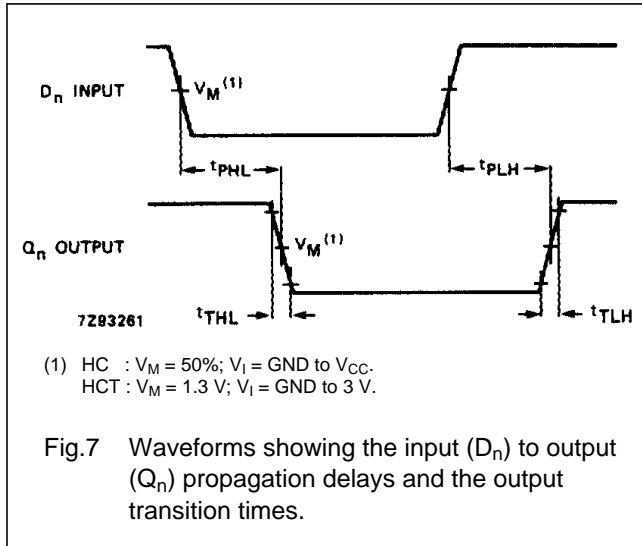
GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

| SYMBOL | PARAMETER | T _{amb} (°C) | | | | | | | | UNIT | TEST CONDITIONS | |
|-------------------------------------|--|-----------------------|------|------|------------|------|-------------|------|----|------|------------------------|-----------|
| | | 74HCT | | | | | | | | | V _{CC} (V) | WAVEFORMS |
| | | +25 | | | -40 to +85 | | -40 to +125 | | | | | |
| | | min. | typ. | max. | min. | max. | min. | max. | | | | |
| t _{PHL} / t _{PLH} | propagation delay D _n to Q _n | | 17 | 30 | | 38 | | 45 | ns | 4.5 | Fig.7 | |
| t _{PHL} / t _{PLH} | propagation delay LE to Q _n | | 16 | 32 | | 40 | | 48 | ns | 4.5 | Fig.8 | |
| t _{PZH} / t _{PZL} | 3-state output enable time \overline{OE} to Q _n | | 19 | 32 | | 40 | | 48 | ns | 4.5 | Fig.9 | |
| t _{PHZ} / t _{PLZ} | 3-state output disable time \overline{OE} to Q _n | | 18 | 30 | | 38 | | 45 | ns | 4.5 | Fig.9 | |
| t _{THL} / t _{TLH} | output transition time | | 5 | 12 | | 15 | | 18 | ns | 4.5 | Fig.7 | |
| t _W | LE pulse width HIGH | 16 | 4 | | 20 | | 24 | | ns | 4.5 | Fig.8 | |
| t _{SU} | set-up time D _n to LE | 12 | 6 | | 15 | | 18 | | ns | 4.5 | Fig.10 | |
| t _H | hold time D _n to LE | 4 | -1 | | 4 | | 4 | | ns | 4.5 | Fig.10 | |

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AC WAVEFORMS



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PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.